



PATENT ABSTRACTS OF JAPAN

(11) Publication number: 06224440 A

(43) Date of publication of application: 12.08.1994

(51) Int. Cl. H01L 29/788
H01L 29/792(21) Application number: 05027463
(22) Date of filing: 21.01.1993(71) Applicant: NIPPON STEEL CORP
(72) Inventor: IWASA SHOICHI(54) MOS FIELD-EFFECT TRANSISTOR AND
NONVOLATILE SEMICONDUCTOR MEMORY
DEVICE

(57) Abstract:

PURPOSE: To provide a MOS field-effect transistor and a nonvolatile semiconductor memory device in which the number of crystal defects is very few and an erase efficiency is excellent and it is useful for fineness because of a short channel length and a punch through is very difficult to occur and a contact resistance is low.

CONSTITUTION: A MOS field-effect transistor comprises a pair of first polycrystalline silicon layers 14 of a second conductivity type which are formed on active regions respectively isolated by isolation insulating films 12 on a semiconductor substrate 11 of a first conductivity type and are mutually separated at a minute

distance, diffusion layers 19 of the second conductivity type formed on the entire active regions of the semiconductor substrate 11 in contact with the bottom of the first polycrystalline silicon layers 14 and the circumference of the active regions, a gate insulating film 13 formed on the first polycrystalline silicon layers 14 and the active regions, and a gate electrode 18 formed on the gate insulating film 13.

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